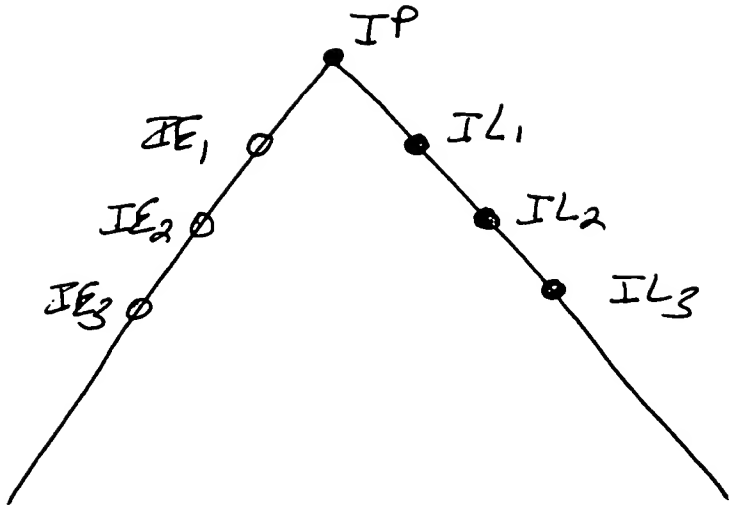


FIGURE 1

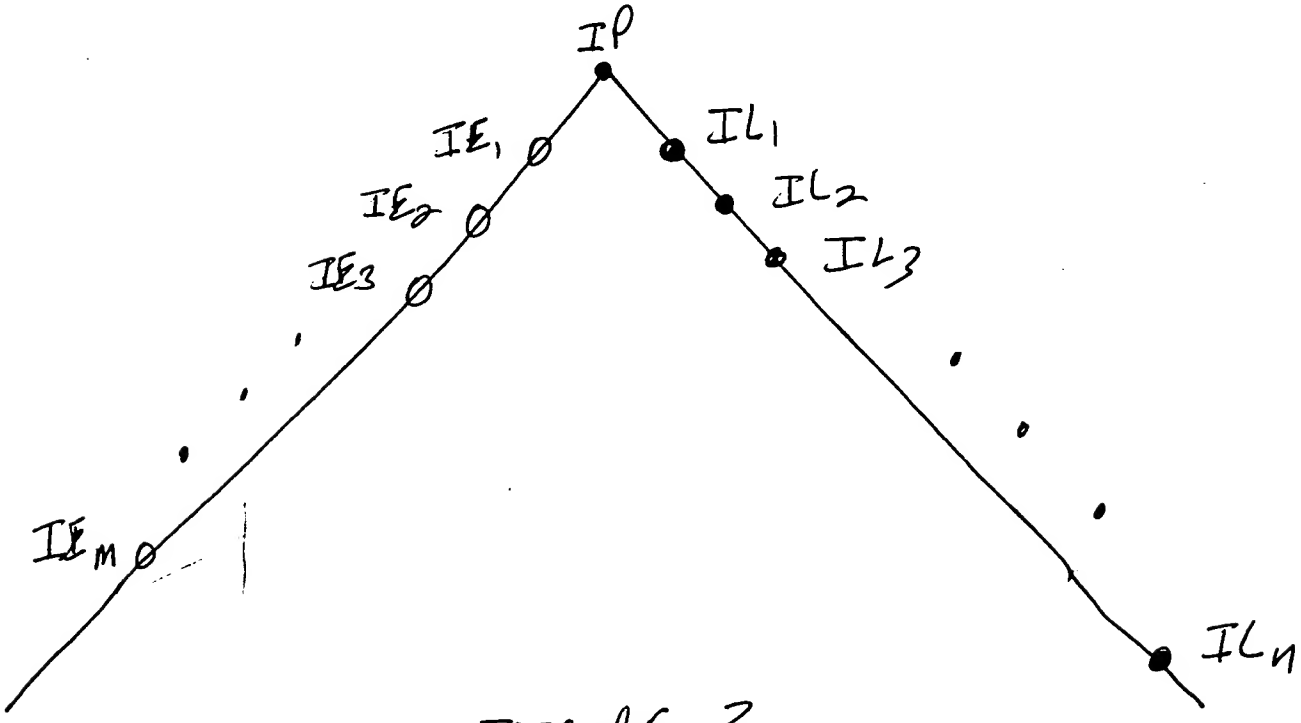
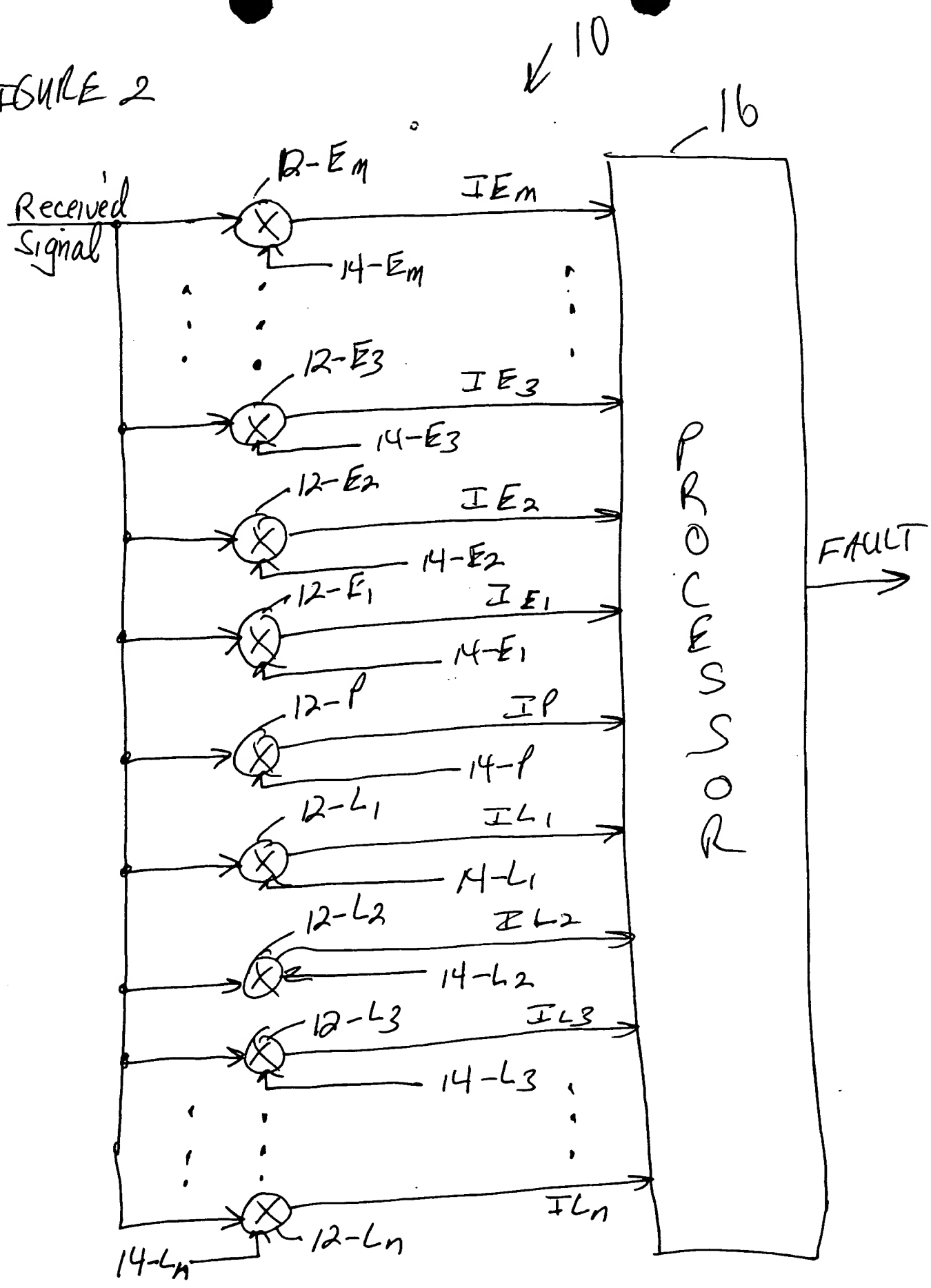


FIGURE 3

FIGURE 2


10
16
Received Signal
12-Em
IEm
14-Em
12-E3
IE3
14-E3
12-E2
IE2
14-E2
12-E1
IE1
14-E1
12-P
IP
14-P
12-L1
IL1
14-L1
12-L2
IL2
14-L2
12-L3
IL3
14-L3
ILn
12-Ln
14-Ln
PROCESSOR
FAULT